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EXAMINER	
SKED, MATTHEW J	
ART UNIT	**PAPER NUMBER**
2655	

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/009,244	NOMURA, TOSHIYUKI	
	Examiner	Art Unit	
	Matthew J Sked	2655	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 December 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/6/01, 5/22/02, 3/26/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The specification on page 13, lines 4-5 refers to P.P. Vaidyanathan "Multirate Systems and Filter Banks" but this is not included in any of the Information Disclosure Statement. The listing of references in the specification is not a proper information disclosure statements. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

2. Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1, 4, 7, and 9 are objected to because of the following informalities: "signal" in the second line of each claim should be changed to –signals--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 7 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification filed 12/06/01. In that paper, applicant has stated on page 16, lines 13-17 that "The addition circuit weights/adds the first speech signal having undergone sampling frequency conversion and the second speech signal having undergone delay adjustment, and outputs the resultant signal to the switching circuit", and this statement indicates that the invention is different from what is defined in the claim(s) because the claim does not specify the addition step that follows the weighting of the two signals in order to produce an output signal to be applied to the switching circuit.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant states "said plurality of sampling frequency

conversion circuits", however claim 1 does not mention a plurality of frequency conversion circuits. For examination it will be assumed that claim 14 should depend on claim 4.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ema et al. (U.S. Pat. 6,094,638) in view of Morrison (U.S. Pat. 5,809,472).

As per claim 1, Ema teaches a speech apparatus for receiving a plurality of input signals sampled with a plurality of different sampling frequencies comprising:

at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals (col. 5, lines 52-64); and

mixing the audio signals by using a time division multiplex method (col. 6, lines 27-36).

Ema teaches a delay adjustment circuit for adjusting a phase of the remaining input signals and outputting the signal (delay circuit setting the audio data signals in phase, col. 5, lines 65 through col. 6 line 9) but does not teach adjusting the phase of

the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention for the delay adjustment circuit to adjust both the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and the phase of the remaining input signal because it would delay the signals to a specific phase which could be used to in a further synchronization such as with a video signal.

Ema does not teach a switching circuit for selecting one of a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Morrison teaches a switching circuit for selecting one of a plurality of output signals in accordance with the control signal (identification signal used to control the switching circuit which switches between the wideband and narrowband signals, col. 8, lines 1-23 and Fig. 3, element 76 and 78).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the audio signals using the switching circuit as taught by Morrison instead of the time division multiplex method taught by Ema because time division multiplexing wastes channel capacity hence switching is more efficient.

9. As per claim 2, Ema teaches that said delay adjustment circuit makes an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal (sets the audio signals in phase, col. 6, lines 5-7).

10. As per claim 3, Ema does not teach that the switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by the control signal.

Morrison teaches the switching circuit switches outputs at a timing set with respect to a switching timing designated by the control signal (switch functions in response to the identification signal which contains block timing information, col. 8, lines 18-23 and col. 7, lines 45-49).

Neither Ema nor Morrison specifically teach that the switching circuit switches outputs at a timing set in consideration of a delay timing in said delay adjustment circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema so that the switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by a control signal because using a control signal is a well known and simple technique to control the timing of a switch, and the control signal would not otherwise take into account the delay operation that would be performed on the signals at the decoder, hence this delay would need to be taken into consideration during switching to give a smooth intermingled output signal.

11. As per claim 4, Ema teaches a speech apparatus for receiving a plurality of input signals sampled with a plurality of different sampling frequencies comprising:

a plurality of sampling frequency conversion circuits for converting a sampling frequency of at least one of the plurality of input signals (multiple frequency converting circuits, col. 8, 50-56 and Fig. 4, element 71B); and

a delay adjustment circuit for adjusting phases between output signals from said plurality of sampling frequency circuits and the remaining input signals (col. 9, lines 6-19).

Ema does not teach adjusting the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention for the delay adjustment circuit to adjust both the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and the phase of the remaining input signal because it would delay the signals to a specific phase which could be used to in a further synchronization such as with a video signal.

Ema teaches mixing the audio signals by using a time division multiplex method (col. 6, lines 27-36).

Ema does not teach a switching circuit for selecting one of a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Morrison teaches a switching circuit for selecting one of a plurality of output signals in accordance with the control signal (identification signal used to control the switching circuit which switches between the wideband and narrowband signals, col. 8, lines 1-23 and Fig. 3, element 78).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the audio signals using the switching circuit as taught by Morrison

instead of the time division multiplex method taught by Ema because time division multiplexing wastes channel capacity hence switching is more efficient.

12. As per claim 5, Ema teaches that said delay adjustment circuit makes an adjustment to match the phase of the signal whose sampling frequency is converted to the phase of the remaining input signal (sets the audio signals in phase, col. 6, lines 5-7).

13. As per claim 6, Ema does not teach that the switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by the control signal.

Morrison teaches the switching circuit switches outputs at a timing set with respect to a switching timing designated by the control signal (switch functions in response to the identification signal which contains block timing information, col. 8, lines 18-23 and col. 7, lines 45-49).

Neither Ema nor Morrison specifically teach that the switching circuit switches outputs at a timing set in consideration of a delay timing in said delay adjustment circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema so that the switching circuit switches outputs at a timing set in consideration of a delay time in said delay adjustment circuit with respect to a switching timing designated by a control signal because using a control signal is a well known and simple technique to control the timing of a switch, and the control signal would not otherwise take into account the delay operation that would be performed on

the signals at the decoder, hence this delay would need to be taken into consideration during switching to give a smooth intermingled output signal.

14. As per claim 11, Ema teaches that said apparatus further comprises a speech decoding circuit for decoding a plurality of signals sampled from one bit stream with different sampling frequencies, and outputting the signals as the plurality of input signals to said sampling frequency conversion circuit or said delay adjustment circuit (decoder along with audio data generating circuit decodes the audio information and generates the audio data signals and applies them to the frequency conversion circuit and the delay circuit, col. 5, lines 41-44, Fig. 1, element 40, and Fig. 2, element 51).

Ema teaches that one signal is selected from a plurality of output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception (selects the signals with a 48KHz sampling frequency for frequency conversion, col. 5, lines 52-64).

Ema does not teach selecting a signal from the decoder based upon a control signal.

Morrison teaches selecting a signal from the decoder based on a control signal (uses a control signal to operate a switch to select signals from the vocoder, Fig. 3, elements 76, 78, and 82).

It would have been obvious to one of ordinary skill in the art at the time of invention to select from a plurality of output decoded signals from said speech decoding circuit in accordance with both a bit rate at the time of reception and a control signal

because the control signal would need to be modified by using the bit rate in order to acquire the timing information necessary to smoothly intermingle the signals.

15. As per claim 12, Ema teaches that said apparatus further comprises a speech decoding circuit for decoding a plurality of signals sampled from one bit stream with different sampling frequencies, and outputting the signals as the plurality of input signals to said plurality of sampling frequency conversion circuits (decoder along with audio data generating circuit decodes the audio information and generates the audio data signals and apply them to the frequency conversion circuit, col. 5, lines 41-44, Fig. 1, element 40, Fig. 2, element 51, and Fig. 4, element 71B).

Ema teaches that one signal is selected from a plurality of output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception (selects the signals with a 48KHz sampling frequency for frequency conversion, col. 5, lines 52-64).

Ema does not teach selecting a signal from the decoder based upon a control signal.

Morrison teaches selecting a signal from the decoder based on a control signal (uses a control signal to operate a switch to select signals from the vocoder, Fig. 3, elements 76, 78, and 82).

It would have been obvious to one of ordinary skill in the art at the time of invention to select from a plurality of output decoded signals from said speech decoding circuit in accordance with both a bit rate at the time of reception and a control signal

because the control signal would need to be modified by using the bit rate in order to acquire the timing information necessary to smoothly intermingle the signals.

16. As per claim 13, Ema teaches a switching circuit for receiving bit streams obtained by multiplexing a plurality of bit streams in a plurality of types of signals having different sampling frequencies, and switching/outputting the bit streams to a plurality of output terminals in accordance with types of bit streams and outputs to said sampling frequency conversion circuit or delay adjustment circuit (audio data signal generating circuit receives a bit streams and generates multiple audio data signals with different sampling rates and outputs them, col. 5, lines 41-51 and Fig. 2, element 51); and

a decoding circuit for decoding the bit stream prior to the stream switching circuit (audio data signal generating circuit processes bit stream output from the decoder, col. 5, lines 41-45).

Ema does not teach using a plurality of decoders to decode the multiple bit streams output from the bit stream switching circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema to use the bit stream switching circuit prior to decoding and using multiple decoders because it would significantly increase the speed of the system to use more decoders on the same bit stream.

Ema teaches that one signal is selected from a plurality of output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception (selects the signals with a 48KHz sampling frequency for frequency conversion, col. 5, lines 52-64).

Ema does not teach selecting a signal from the decoder based upon a control signal.

Morrison teaches selecting a signal from the decoder based on a control signal (uses a control signal to operate a switch to select signals from the vocoder, Fig. 3, elements 76, 78, and 82).

It would have been obvious to one of ordinary skill in the art at the time of invention to select from a plurality of output decoded signals from said speech decoding circuit in accordance with both a bit rate at the time of reception and a control signal because the control signal would need to be modified by using the bit rate in order to acquire the timing information necessary to smoothly intermingle the signals.

17. As per claim 14, Ema teaches a switching circuit for receiving bit streams obtained by multiplexing a plurality of bit streams in a plurality of types of signals having different sampling frequencies, and switching/outputting the bit streams to a plurality of output terminals in accordance with types of bit streams and outputs to said sampling frequency conversion circuit or delay adjustment circuit (audio data signal generating circuit receives a bit streams and generates multiple audio data signals with different sampling rates and outputs them, col. 5, lines 41-51 and Fig. 2, element 51); and

a decoding circuit for decoding the bit stream prior to the stream switching circuit (audio data signal generating circuit processes bit stream output from the decoder, col. 5, lines 41-45).

Ema does not teach using a plurality of decoders to decode the multiple bit streams output from the bit stream switching circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema to use the bit stream switching circuit prior to decoding and using multiple decoders because it would significantly increase the speed of the system to use more decoders on the same bit stream.

Ema teaches that one signal is selected from a plurality of output decoded signals from said speech decoding circuit in accordance with a bit rate at the time of reception (selects the signals with a 48KHz sampling frequency for frequency conversion, col. 5, lines 52-64).

Ema does not teach selecting a signal from the decoder based upon a control signal.

Morrison teaches selecting a signal from the decoder based on a control signal (uses a control signal to operate a switch to select signals from the vocoder, Fig. 3, elements 76, 78, and 82).

It would have been obvious to one of ordinary skill in the art at the time of invention to select from a plurality of output decoded signals from said speech decoding circuit in accordance with both a bit rate at the time of reception and a control signal because the control signal would need to be modified by using the bit rate in order to acquire the timing information necessary to smoothly intermingle the signals.

18. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ema in view of Morrison and taken in further view of Grill et al. (U.S. Pat. 6,370,507).

As per claim 7, Ema teaches a speech apparatus for receiving a plurality of input signals sampled with a plurality of different sampling frequencies comprising:

at least one sampling frequency conversion circuit for converting a sampling frequency of at least one of the plurality of input signals (col. 5, lines 52-64); and

a delay adjustment circuit for adjusting a phase of the remaining input signal and outputting the signal (delay circuit, col. 5, lines 65 through col. 6 line 9).

Ema does not teach adjusting the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention for the delay adjustment circuit to adjust both the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and the phase of the remaining input signal because it would delay the signals to a specific phase which could be used to in a further synchronization such as with a video signal.

Ema teaches mixing the audio signals by using a time division multiplex method (col. 6, lines 27-36).

Ema does not teach a switching circuit for selecting one of a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Morrison teaches a switching circuit for selecting one of a plurality of output signals in accordance with the control signal (identification signal used to control the switching circuit which switches between the wideband and narrowband signals, col. 8, lines 1-23 and Fig. 3, element 78).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the audio signals using the switching circuit as taught by Morrison

instead of the time division multiplex method taught by Ema because time division multiplexing wastes channel capacity hence switching is more efficient.

Neither Ema nor Morrison teach an addition circuit for selecting, weighting, and adding two signals from a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Grill teaches a decoding method that includes an adding circuit outputting the resultant signal to the switching circuit for adding two signals outputted from the delay adjustment circuit (col. 10, lines 2-6, 20-25, 33-38 and Fig. 2, element 48, 60 and 62), but does not teach weighting the signals prior to adding them and selecting the signals based on the control signal.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema and Morrison to have an addition circuit for adding two signals from a plurality of output signals from said delay adjustment as taught by Grill, to weight the signals prior to adding them and selecting the signals based on the control signal because it would enable the system to choose a corresponding signal with a more appropriate gain. Selecting the signals based on the control signal is obvious because the control signal contains the timing information of the signal therefore using this information would synchronize the adding circuit and the switching circuit.

19. As per claim 8, Ema, Morrison and Grill do not teach that said switching circuit switches a signal before switching of output signals from said delay adjustment circuit to an output signal from said addition circuit at a timing set in consideration of a delay time

in said delay adjustment circuit from a switching timing designated by the control signal, outputs the output signals from said addition circuit for a predetermined interval, and then outputs the signal after switching.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema, Morrison, and Grill so that said switching circuit switches a signal, before the switching of the output signals from said delay adjustment circuit, to an output signal from said addition circuit at a timing set in consideration of both a delay time in said delay adjustment circuit and from a switching timing designated by the control signal, outputs the output signals from said addition circuit for a predetermined interval, and then outputs the signals from said delay adjustment circuit after switching because it would output a signal at a more desired gain for a time of the user's choosing hence making the system more configurable for the user. Also it would synchronize the timing between the switching circuit and the adding circuit hence improving system performance.

20. As per claim 9, Ema teaches a speech apparatus for receiving a plurality of input signals sampled with a plurality of different sampling frequencies comprising:

a plurality of sampling frequency conversion circuits for converting a sampling frequencies of at least one of the plurality of input signals to a predetermined frequency (multiple frequency converting circuits, col. 8, 50-56 and Fig. 4, element 71B); and

a delay adjustment circuit for adjusting phases between output signals from said plurality of sampling frequency circuits and the remaining input signals (col. 9, lines 6-19).

Ema does not teach adjusting the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit.

It would have been obvious to one of ordinary skill in the art at the time of invention for the delay adjustment circuit to adjust both the phase of the plurality of input signals whose sampling frequency is converted by said sampling frequency conversion circuit and the phase of the remaining input signal because it would delay the signals to a specific phase which could be used to in a further synchronization such as with a video signal.

Ema teaches mixing the audio signals by using a time division multiplex method (col. 6, lines 27-36).

Ema does not teach a switching circuit for selecting one of a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Morrison teaches a switching circuit for selecting one of a plurality of output signals in accordance with the control signal (identification signal used to control the switching circuit which switches between the wideband and narrowband signals, col. 8, lines 1-23 and Fig. 3, element 78).

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the audio signals using the switching circuit as taught by Morrison instead of the time division multiplex method taught by Ema because time division multiplexing wastes channel capacity hence switching is more efficient.

Neither Ema nor Morrison teach an addition circuit for selecting, weighting, and adding two signals from a plurality of output signals from said delay adjustment circuit in accordance with the control signal.

Grill teaches a decoding method that includes an adding circuit outputting the resultant signal to the switching circuit for adding two signals outputted from the delay adjustment circuit (col. 10, lines 2-6, 20-25, 33-38 and Fig. 2, element 48, 60 and 62), but does not teach weighting the signals prior to adding them and selecting the signals based on the control signal.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema and Morrison to have an addition circuit for adding two signals from a plurality of output signals from said delay adjustment as taught by Grill, to weight the signals prior to adding them and selecting the signals based on the control signal because it would enable the system to choose a corresponding signal with a more appropriate gain. Selecting the signals based on the control signal is obvious because the control signal contains the timing information of the signal therefore using this information would synchronize the adding circuit and the switching circuit.

21. As per claim 10, Ema, Morrison and Grill do not teach that said switching circuit switches a signal before switching of output signals from said delay adjustment circuit to an output signal from said addition circuit at a timing set in consideration of a delay time in said delay adjustment circuit from a switching timing designated by the control signal,

outputs the output signals from said addition circuit for a predetermined interval, and then outputs the signal after switching.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the system of Ema, Morrison, and Grill so that said switching circuit switches a signal, before the switching of the output signals from said delay adjustment circuit, to an output signal from said addition circuit at a timing set in consideration of both a delay time in said delay adjustment circuit and from a switching timing designated by the control signal, outputs the output signals from said addition circuit for a predetermined interval, and then outputs the signals from said delay adjustment circuit after switching because it would output a signal at a more desired gain for a time of the user's choosing hence making the system more configurable for the user. Also it would synchronize the timing between the switching circuit and the adding circuit hence improving system performance.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gersho et al. (U.S. Pat. 2001/0023396A1) and Nomura (U.S. Pat. 6,208,957) teach decoders that use switching. Tanaka (U.S. Pat. 6,714,825) and Ejima (U.S. Pat. 6,449,596) teach systems that use frequency conversion circuit in the decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Sked whose telephone number is (703) 305-8663. The examiner can normally be reached on Mon-Fri (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Talivaldis Smits can be reached on (703) 306-3011. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MS
12/29/04

TĀLIVALDIS IVARS ŠMITS
PRIMARY EXAMINER